Large Scale DRAM Model

“DRAM Engineers”

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Client

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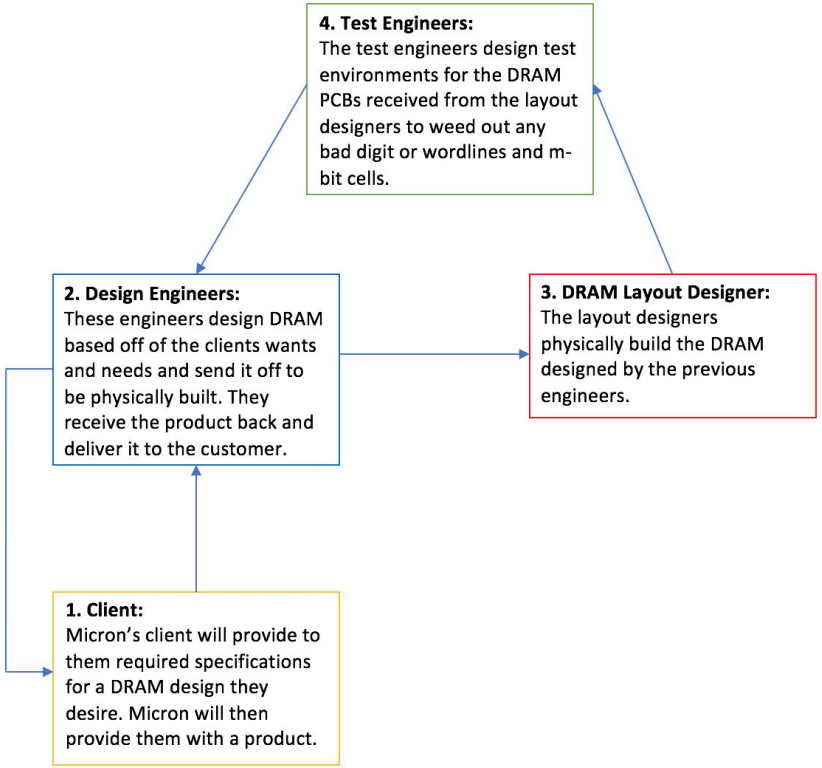
Clients

- Daniel Eichenberger, Micron Test Engineer/Recruiter.
- Engineering Students interested in a career with Micron.
- Need a model to display how a basic DRAM array operates.

Micron DRAM Business Flow Diagram



What is DRAM?

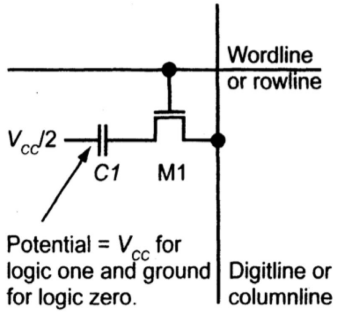
Dynamic Random Access Memory:

- A type of memory used in computers, smartphones, and many modern technologies.
- This form of RAM is Dynamic, meaning it requires a refresh cycle.
- Comprised of an array of individual memory cells, m-bits.
- Our client, Micron is one of the largest DRAM manufacturers in the country.

Why a Large Scale DRAM Model?

- Currently, DRAM operations and functions cannot be simulated with just a DRAM PCB easily.
- Recruiters want an interactive tool to show prospective employees.
- Can also be used to test interviewee’s knowledge of DRAM.

Basic DRAM Operation



The m-bit Cell:

- The main component for storing a bit of memory in the array.
- Comprised of an NMOS transistor with Gate tied to wordline, Drain tied to digitline, and source tied to a storage capacitor.
- Accessed by applying opening up the digitline, selecting the appropriate wordline by applying a small voltage, then the user can read or write to that cell.
- Needs to be refreshed at least every 64ms.

Basic DRAM Operation Cont.

The Peripheral Circuitry:

- Accesses the desired m-bit cell from user and reads the data stored on the m-bit.
- A Sense Amplifier identifies the data in the form of a small signal and amplifies the signal to a readable output.
- Circuitry inside the sense amp keeps digitline and wordline voltages low to prevent accidental access to other cells.

Project/Problem Definition

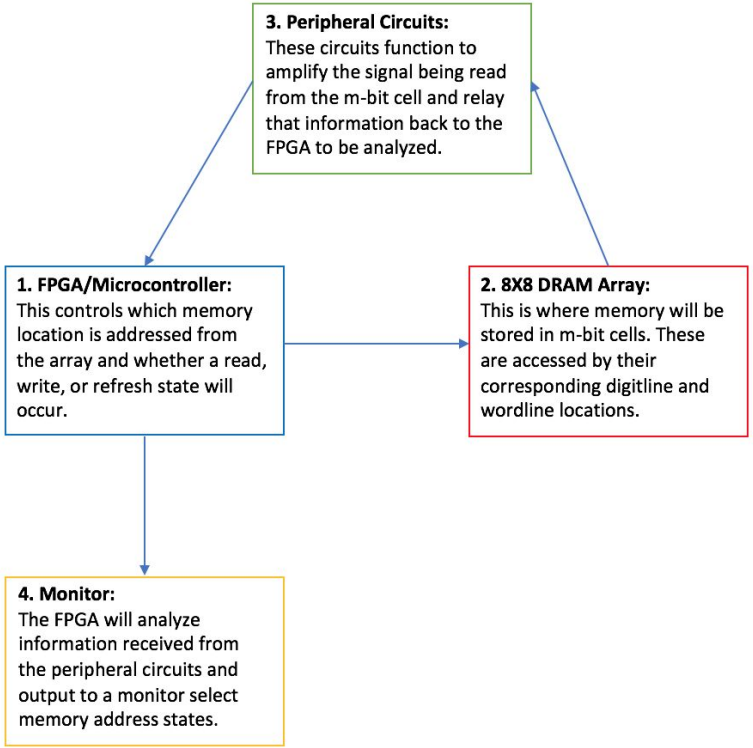
- Develop a large scale model of an 8x8 DRAM array.
- Needs to demonstrate read, write, and refresh cycles.
- Will be shown to prospective Micron employees.
- Currently Micron recruiters use a small DRAM PCB that cannot emulate DRAM operation.

Project Goal

Design and build a large scale DRAM by using:

- Capacitors
- MOSFETs
- LEDs or some display
- Microcontroller or FPGA (Field Programmable Gate Array)

Ideal Project Flow Diagram



Possible Solutions

Possible Microcontrollers/FPGAs:

- Arduino Uno
- Raspberry Pi
- Altera Cyclone V

Possible Display solutions:

- 7-segment displays
- LEDs
- Serial Monitor/LCD Display

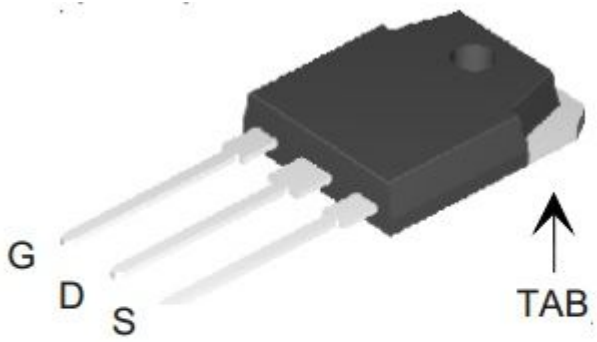
Possible Solutions Cont.

Possible Storage Capacitors:

- Ceramic
- Electrolytic
- Super

Possible Transistors:

- MOSFETs
- BJTs



G = Gate
S = Source
D = Drain
TAB = Drain

Requirements and Specifications

Mechanical:

- Weigh between 0-5 lbs.
- Small enough to carry with one hand.
- Withstand table height drops (3 feet or less).

Electrical:

- 1.2V minimum required to be applied to access the wordline.
- Accurate enough to show different states.

Requirements and Specifications Cont.

Documentation:

- User's guide will be provided by capstone team.

Software:

- Programming languages used will either be C or VHDL.
- Pyxis Mentor Graphics will prototype model.

Environmental:

- Will be stored in a climate controlled room (between 70° - 85° Fahrenheit).

Conclusion

- Design and create an 8x8 DRAM array that simulates read, write, and refresh operations.
- Individual bits of memory can be accessed.
- Charge states, memory locations, and read and write voltages will be displayed.
- Can be transported easily.
- Solves the problem of demonstrating DRAM operations.

Questions?